Customer No.: 31561 Application No.: 10/708,175 Docket No.: 11836-US-PA

## IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with an P-type gate, comprising:

providing a substrate;

forming a gate dielectric layer over the substrate;

forming an indium doped polysilicon layer over the gate dielectric layer by using a chemical vapor deposition process with a gas comprising indium chloride (InCl<sub>3</sub>);

patterning the indium doped polysilicon layer and the gate dielectric layer to form a gate; and

forming an N-doped region in the substrate on each side of the gate.

2. (currently amended) The method of claim 1, wherein a gas source for the introduced indium chloride (InCl<sub>2</sub>) comprises evaporating solid indium chloride (InCl<sub>3</sub>) to form indium chloride vapor before passing the indium chloride vapor into a reaction chamber during the step of forming an indium doped polysilicon layer over the gate dielectric layer comprises performing an in-situ indium-ion doping during a chemical vapor deposition operation process.

## Claims 3-7 (canceled).

8. (currently amended) A method of manufacturing an N-channel metal-oxide semiconductor (NMOS) transistor with a P-type gate, comprising:

providing a substrate;

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forming a gate dielectric layer over the substrate;

performing a chemical vapor deposition process using a gas comprising indium chloride (InCl<sub>3</sub>), SiH4, nitrogen and argon to form forming an indium doped polysilicon layer over the gate dielectric layer, wherein the indium doped polysilicon layer is formed by performing an in-situ doping chemical vapor deposition operation using caseous indium chloride (InCl<sub>2</sub>) as a doping source;

forming a silicide layer over the indium doped polysilicon layer;

patterning the silicide layer, the indium doped polysilicon layer and the gate dielectric layer to form a gate; and

forming an N-doped region in the substrate on each side of the gate.

9. (currently amended) The method of claim 8, wherein the step of forming an doped polysilicon layer over the gate dielectric layer a gas source of the introduced indium chloride (InCl<sub>2</sub>) comprises evaporating the solid indium chloride (InCl<sub>2</sub>) to form indium chloride vapor before passing introducing the indium chloride vapor into a reaction chamber during for conducting the chemical vapor deposition process.

10. (original) The method of claim 9, wherein the step of evaporating solid indium chloride to form a gaseous vapor comprises heating the solid indium chloride to a temperature of about 280°C.

## Claim 11-20 (canceled).

21. (new) The method of claim 1, further comprising a step of forming a silicide layer over the indium doped polysilicon layer.

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22. (new) The method of claim 2, wherein the step of evaporating solid indium chloride to form a gaseous vapor comprises heating the solid indium chloride to a temperature of about 280°C.